WHAT IS CLAIMED IS:

1. A memory apparatus, comprising:

at least one cell array having a plurality of memory cells, each memory cell having an associated word line and an associated bit line;

a control device having a signaling connection to a plurality of word lines and bit lines wherein the control device is configured to execute a destructive read command for reading data from at least one memory cell, the destructive read command comprising:

electrically biasing a bit line associated with the at least one memory cell;

opening a word line associated with the at least one memory cell; and

destructively reading data stored in the at least one memory cell.

2. The memory apparatus of claim 1, wherein the control device is further configured to execute a write command for writing data to at least one memory cell, the write command comprising:

writing data to the at least one memory cell without first reading stored data in the memory cell.

3. The memory apparatus of claim 1, wherein the control device is further configured to execute a nondestructive read command for reading data from at least one of the memory cells, the nondestructive read command comprising:

electrically biasing the bit line associated with the at least one memory cell;

opening the word line associated with the at least one memory cell;

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

4. The memory apparatus of claim 1, wherein the control device is further configured to execute a refresh command for refreshing data stored in at least one memory cell, the refresh command comprising:

electrically biasing the bit line associated with the at least one memory cell;

opening the word line associated with the at least one memory cell;

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

5. The memory apparatus of claim 1, wherein the memory apparatus is a DRAM.

6. The memory apparatus of claim 1, wherein the memory apparatus is an SRAM.

7. The memory apparatus of claim 1, wherein the memory apparatus is a buffer storage device.

8. A method for operating a plurality of memory cells in a memory apparatus, the method comprising:

executing a destructive read command for reading data from at least one memory cell, the destructive read command, comprising:

electrically biasing the bit line associated with the at least one memory cell;

opening the word line associated with the at least one memory cell; and

destructively reading data stored in the at least one memory cell.

9. The method of claim 8, further comprising:

executing a destructive write command for writing data from at least one memory cell, the destructive write command comprising:

writing the data to the at least one memory cell without first reading stored data in the memory cell.

10. The method of claim 9, further comprising:

executing a nondestructive read command for reading data from at least one memory cell, the nondestructive read command comprising:

electrically biasing the bit line associated with the at least one memory cell;

opening the word line associated with the at least one memory cell; and

destructively reading data stored in the at least one memory cell; and writing the read data to the at least one memory cell.

11. The method of claim 10, further comprising:

executing a refresh command for refreshing data in at least one memory cell, the refresh command comprising:

electrically biasing the bit line associated with the at least one memory cell;

opening the word line associated with the at least one memory cell; and

destructively reading data stored in the at least one memory cell; and writing the read data to the at least one memory cell.

12. The method of claim 8, further comprising:

executing a nondestructive read command for reading data from at least one memory cell, the nondestructive read command comprising:

electrically biasing the bit line associated with the at least one memory cell;

opening the word line associated with the at least one memory cell; and

destructively reading data stored in the at least one memory cell; and writing the read data to the at least one memory cell.

13. The method of claim 8, further comprising:

executing a refresh command for refreshing data in at least one memory cell, the refresh command comprising:

electrically biasing the bit line associated with the at least one memory cell;

opening the word line associated with the at least one memory cell; and

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

14. A memory apparatus, comprising:

at least one cell array having a plurality of memory cells having associated word lines and associated bit lines;

a control means for executing a destructive read command for reading data from at least one memory cell, the destructive read command comprising:

electrically biasing a bit line associated with the at least one memory cell;

opening a word line associated with the at least one memory cell; and

destructively reading data stored in the at least one memory cell.

15. The memory apparatus of claim 14, wherein the control means is further configured for executing a write command for writing data to at least one memory cell, the write command comprising:

writing data to the at least one memory cell without first reading stored data in the memory cell.

16. The memory apparatus of claim 15, wherein the control means is further configured for executing a nondestructive read command for reading data from at least one of the memory cells, the nondestructive read command comprising:

electrically biasing the bit line associated with the at least one memory cell;

opening the word line associated with the at least one memory cell;

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

17. The memory apparatus of claim 16, wherein the control means is further configured for executing a refresh command for refreshing data stored in at least one memory cell, the refresh command comprising:

electrically biasing the bit line associated with the at least one memory cell;

opening the word line associated with the at least one memory cell;

destructively reading data stored in the at least one memory cell; and

writing the read data to the at least one memory cell.

18. The memory apparatus of claim 17, wherein the memory apparatus is a DRAM.

19. The memory apparatus of claim 17, wherein the memory apparatus is an SRAM.

20. The memory apparatus of claim 17, wherein the memory apparatus is a buffer storage device.